"Lauffer," Wenzel et al. (US 6,150,724), hereafter "Wenzel," and Pogge et al. (US 5,998,868), hereafter "Pogge." This rejection is defective because the cited references, taken alone or in any combination, fail to teach or suggest each and every feature of the present invention as required by 35 U.S.C. §103. In addition, the Examiner has failed to present a *prima facie* case of obviousness in support of the rejection under 35 U.S.C. §103.

Claim 1 recites:

4

"A multiple semiconductor chip (multi-chip) module, comprising at least a power semiconductor chip and a control semiconductor chip each mounted directly on an electrically conductive heat sink, wherein said power semiconductor chip comprises a Silicon-On-Insulator (SOI) device and said control semiconductor ship comprises a bulk technology semiconductor device having no insulating layer between a device layer and a substrate thereof, and having said substrate connected to ground potential, and said power semiconductor chip and said control semiconductor chip are directly mounted on said electrically conductive heat sink without the use of a separate electrical insulation layer."

Takagi fails to teach or suggest, among other features, a multi-chip module "comprising at least a power semiconductor chip and a control semiconductor chip each mounted directly on an electrically conductive heat sink," wherein "said power semiconductor chip comprises a Silicon-On-Insulator (SOI) device and said control semiconductor ship comprises a bulk technology semiconductor device having no insulating layer between a device layer and a substrate thereof." On the contrary, in Takagi, a power element chip 200 and a control circuit chip 100, both formed using SOI technology, are mounted on a conductive substrate (see, e.g.,

Serial No.: 09/440,595

FIGS. 12A, 12B; col. 11, line 30-col. 12, line 57). In order to overcome this glaring deficiency of Takagi, the Examiner presents a convoluted argument involving the disparate teachings of Lauffer, Wenzel and Pogge in an attempt to prove that "it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a control semiconductor chip comprising a bulk technology device and an electrically conductive heat sink substrate connected to ground potential as taught by Lauffer et al, Wenzel et al and Pogge et al so that heat dissipation, temperature distribution and power requirements can be improved in Takagi et al's multichip module." Applicants respectfully disagree with the Examiner's analysis and conclusion.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Applicants submit that there is no suggestion or motivation to modify Takagi in the manner suggested by the Examiner.

Takagi discloses the formation of monolithic and hybrid power integrated circuits (IC's) using SOI technology. In particular, Takagi discloses a plurality of different embodiments of SOI power IC's, each including SOI control and power structures/chips that have been specifically designed to prevent/inhibit the problems of latchup and leakage current present in

Serial No.: 09/440,595

٤

١

3

IC's, and is not concerned in any way with bulk semiconductor devices. As such, one of ordinary skill in the art would not be motivated to modify Takagi to include a control circuit chip

prior art SOI power IC's. Takagi is concerned only with problems associated with SOI power

formed using a bulk semiconductor technology as asserted by the Examiner. Indeed, this

modification would likely render Takagi inoperable for its specific intended purpose, i.e., the

prevention of latchup and the reduction of leakage current present in prior art SOI power IC's.

The remaining references cited by the Examiner do not remedy the substantial deficiencies of Takagi.

Accordingly, because the cited references, taken alone or in any combination, fail to teach each and every feature of claim 1, Applicants respectfully submit that claim 1 is allowable.

Claims 2-7 depend from independent claim 1, and are, therefore, patentable for at least the reasons set forth above.

If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

Ronald A. D'Alessandro, Jr.

Reg. No. 42,456

Hoffman, Warnick & D'Alessandro LLC

Three E-Comm Square

Dated: 6/11/03

Albany, NY 12207

(518) 449-0044 - Telephone

(518) 449-0047 - Facsimile

4